L Number	Hits	Search Text	DB	Time stamp
1	12597	leadframe lead! adj frame	USPAT; US-PGPUB	2002/12/11 20:38
2	3292	(tin! sn!) adj (cu! copper!)	USPAT; US-PGPUB	2002/12/11 20:39
3	61674	solder	USPAT; US-PGPUB	2002/12/11 20:39
4	31	((tin! sn!) adj (cu! copper!)) adj solder	USPAT; US-PGPUB	2002/12/11 20:39
5	2	(((tin! sn!) adj (cu! copper!)) adj solder) with thick$	USPAT; US-PGPUB	2002/12/11 20:40
6	2	(leadframe lead! adj frame) and ((((tin! sn!) adj (cu! copper!)) adj solder) with thick$)	USPAT; US-PGPUB	2002/12/11 20:42
7	242	((tin! sn!) adj (cu! copper!)) with solder	USPAT; US-PGPUB	2002/12/11 20:42
8	17	(((tin! sn!) adj (cu! copper!)) with solder) with thick$	USPAT; US-PGPUB	2002/12/11 20:43
9	3	((((tin! sn!) adj (cu! copper!)) with solder) with thick$) and (leadframe lead! adj frame)	USPAT; US-PGPUB	2002/12/11 20:43
10	11	((tin! sn!) adj (cu! copper!)) with (leadframe lead! adj frame)	USPAT; US-PGPUB	2002/12/11 20:44
11	2	(((tin! sn!) adj (cu! copper!)) with (leadframe lead! adj frame)) with (thick$ thin$)	USPAT; US-PGPUB	2002/12/11 20:45
12	6	(((tin! sn!) adj (cu! copper!)) adj solder) and (leadframe lead! adj frame)	USPAT; US-PGPUB	2002/12/11 21:18
13	172	(leadframe lead! adj frame) near3 thick	USPAT; US-PGPUB	2002/12/11 20:50
14	323177	@ad>20000713 @rlad>20000713	USPAT; US-PGPUB	2002/12/11 20:51
15	148	((leadframe lead! adj frame) near3 thick) not (@ad>20000713 @rlad>20000713)	USPAT; US-PGPUB	2002/12/11 21:17
16	3	(((leadframe lead! adj frame) near3 thick) not (@ad>20000713 @rlad>20000713)) and ((tin! sn!) adj (cu! copper!))	USPAT; US-PGPUB	2002/12/11 20:52
17	20	(pd palladium) and (((leadframe lead! adj frame) near3 thick) not (@ad>20000713 @rlad>20000713))	USPAT; US-PGPUB	2002/12/11 20:56
18	242	((tin! sn!) adj (cu! copper!)) with solder	USPAT; US-PGPUB	2002/12/11 21:18
19	36	(((tin! sn!) adj (cu! copper!)) with solder) and (leadframe lead! adj frame)	USPAT; US-PGPUB	2002/12/11 21:18
20	16	((((tin! sn!) adj (cu! copper!)) with solder) and (leadframe lead! adj frame)) not (@ad>20000713 @rlad>20000713)	USPAT; US-PGPUB	2002/12/11 21:18
-	1	("6376901").PN.	USPAT; US-PGPUB	2002/12/06 15:48
-	9910	(nickel nickle ni) with (palladium pd) with (silver ag)	USPAT; US-PGPUB	2002/12/06 15:50
-	2454	lead! adj free!	USPAT; US-PGPUB	2002/12/06 15:50
-	6	((nickel nickle ni) with (palladium pd) with (silver ag)) with (lead! adj free!)	USPAT; US-PGPUB	2002/12/06 17:21

-	61571	solder	USPAT; US-PGPUB	2002/12/06 16:17
-	180	solder with ((nickel nickle ni) with (palladium pd) with (silver ag))	USPAT; US-PGPUB	2002/12/06 16:17
-	320939	@ad>20000713 @rlad>20000713	USPAT; US-PGPUB	2002/12/06 16:22
-	35	(solder with ((nickel nickle ni) with (palladium pd) with (silver ag))) and (leadframe lead! adj frame)	USPAT; US-PGPUB	2002/12/06 16:27
-	19	((solder with ((nickel nickle ni) with (palladium pd) with (silver ag))) and (leadframe lead! adj frame)) not (@ad>20000713 @rlad>20000713)	USPAT; US-PGPUB	2002/12/06 16:27
-	379	(palladium pd) with (silver ag) with solder!	USPAT; US-PGPUB	2002/12/06 17:22
-	73	(leadframe lead! adj frame) and ((palladium pd) with (silver ag) with solder!)	USPAT; US-PGPUB	2002/12/06 17:22
-	43	((leadframe lead! adj frame) and ((palladium pd) with (silver ag) with solder!)) not (@ad>20000713 @rlad>20000713)	USPAT; US-PGPUB	2002/12/06 17:46
-	16	("3648355" | "4141029" | "4404080" | "4405432" | "4441118" | "4486511" | "4529667" | "4628165" | "4888449" | "4894752" | "5001546" | "5138431" | "5221859" | "5360991" | "5454929" | "5486721").PN.	USPAT	2002/12/06 17:36
-	2985	(silver ag) adj coated	USPAT; US-PGPUB	2002/12/06 17:46
-	21	(leadframe lead! adj frame) with ((silver ag) adj coated)	USPAT; US-PGPUB	2002/12/06 17:46
-	20	((leadframe lead! adj frame) with ((silver ag) adj coated)) not (@ad>20000713 @rlad>20000713)	USPAT; US-PGPUB	2002/12/06 18:02
-	4	((silver ag) adj coated) with (palladium pd) with (nickle ni)	USPAT; US-PGPUB	2002/12/06 18:02
-	1	(((silver ag) adj coated) with (palladium pd) with (nickle ni)) and (leadframe lead! adj frame)	USPAT; US-PGPUB	2002/12/06 18:55
-	22	4529667.URPN.	USPAT	2002/12/06 18:07
-	408	spot! adj (plate plated plating)	USPAT; US-PGPUB	2002/12/06 18:56
-	116446	palladium pd	USPAT; US-PGPUB	2002/12/06 18:56
-	22	(palladium pd) with (spot! adj (plate plated plating))	USPAT; US-PGPUB	2002/12/06 18:56
-	19	((palladium pd) with (spot! adj (plate plated plating))) and (leadframe lead! adj frame)	USPAT; US-PGPUB	2002/12/06 18:56
-	13	(((palladium pd) with (spot! adj (plate plated plating))) and (leadframe lead! adj frame)) not (@ad>20000713 @rlad>20000713)	USPAT; US-PGPUB	2002/12/09 17:44
-	5	(("4529667") or ("re34227") or ("5454929") or ("5728285") or ("6352634")).PN.	USPAT; US-PGPUB	2002/12/11 15:53

-	3665	inner! adj lead	USPAT; US-PGPUB	2002/12/11 15:53
-	3178	outer! adj lead	USPAT; US-PGPUB	2002/12/11 15:53
-	24	(inner! adj lead) with (pd palladium)	USPAT; US-PGPUB	2002/12/11 16:49
-	136	(outer! adj lead) with (sn tin)	USPAT; US-PGPUB	2002/12/11 15:54
-	5	((inner! adj lead) with (pd palladium)) and ((outer! adj lead) with (sn tin))	USPAT; US-PGPUB	2002/12/11 16:30
-	3	("4068022" | "5360991" | "5436082").PN.	USPAT	2002/12/11 16:18
-	545	(outer! adj lead) with solder	USPAT; US-PGPUB	2002/12/11 16:30
-	11	((outer! adj lead) with solder) and ((inner! adj lead) with (pd palladium))	USPAT; US-PGPUB	2002/12/11 16:31
-	7	(((outer! adj lead) with solder) and ((inner! adj lead) with (pd palladium))) not (((inner! adj lead) with (pd palladium)) and ((outer! adj lead) with (sn tin)))	USPAT; US-PGPUB	2002/12/11 16:31
-	5	("4942454" | "5041901" | "5455446" | "5616953" | "5994767").PN.	USPAT	2002/12/11 16:45
-	12	((inner! adj lead) with (pd palladium)) not ((((inner! adj lead) with (pd palladium)) and ((outer! adj lead) with (sn tin))) (((outer! adj lead) with solder) and ((inner! adj lead) with (pd palladium))))	USPAT; US-PGPUB	2002/12/11 16:50

US-PAT-NO: 5497032

DOCUMENT-IDENTIFIER: US 5497032 A

TITLE: Semiconductor device and lead frame therefore

---------- KWIC ---------

In step ST2, a plating process is performed in which the aforementioned SnNi protection film is coated on the outer leads 257b. Further, at least the end portions of the **inner leads** 253a and the chip-mounting-side surfaces of the second and third areas 253b and 253c are plated with a metallic film suitable for wire bonding, such as silver (Ag), gold (Au) or **palladium (Pd)**.

In step ST15, the back surface of the stage 253 exposed from the package 259 is removed by a chemical etching process until the half-etched grooves 253 appear. Thereby, as shown in FIG. 17C, the first, second and third areas 253a, 253b and 253c are completely separated from each other by the resin. In the above chemical etching process, the assembly is placed in an etchant. It will be noted that the outer leads 257b are plated with SnNi and the outer leads 257b are not etched. In step ST16, the **outer leads** 257b are plated with **solder**. In step ST17, the outer leads 257b are bent in the gull-wing shape.

FIG. 20 is a diagram of a method of producing the semiconductor device 251B shown in FIG. 19. In FIG. 20, steps which are the same as those shown in FIGS. 18A and 18B are given the same reference numbers as previously, and a description thereof will be omitted. In step S13 shown in

FIG. 20, only wires connecting the semiconductor chip 254 to the second and third stage areas 253b and 253c are provided because the semiconductor device 251B employs the bump electrodes 260. The bump electrodes 260 are provided in step ST16.sub.A subsequent to step ST16 in which the **outer leads** 257b are plated with **solder**. After step ST16.sub.A, step S17 is performed.

In step ST25, the end portions of the **inner leads** 257a1-257a8 are plated with Ag, Au or **Pd**. The portions corresponding to the outer leads 257b are plated with SnNi in order to improve the anti-etching performance. In step ST26, the stage-part frame 252A and the lead-part frame 252B are stacked so that the end portions of the signal-system inner leads 257a3 adhere to the top of the insulating adhesive tape 263. In step ST27, the insulating adhesive tape 265 is cured whereby the inner leads 257a3 are fixed to the insulating adhesive tape 265. Then, by using the lead frame 252 thus formed, the semiconductor device 251E is produced in the same manner as shown in FIG. 18B.

US-PAT-NO: 5744868

DOCUMENT-IDENTIFIER: US 5744868 A

TITLE: Encapsulated electronic component having a plurality of connection
leads of martensitic structural-hardening conductive alloy

---------- KWIC ---------

The connection leads are, optionally, coated with a galvanic deposition of
nickel and then gold, **silver or palladium,** and their external parts may be
tinned or include a deposition of **solder**.

US-PAT-NO: 5138431

DOCUMENT-IDENTIFIER: US 5138431 A

TITLE: Lead and socket structures with reduced self-inductance

---------- KWIC ---------

In conventional leadframe manufacturing, Alloy 42 leadframes have been plated with aluminum, gold or silver to provide a reliable metallurgical bond to aluminum and gold wires and to provide a wettable surface for quality soldering. Gold over nickel plating of Alloy 42 leadframes was popular until the price of gold approached $800.00 per ounce. When this occurred, spot-plating techniques were developed to plate gold only in the die attach pad and wire bond regions on one side of the leadframe strips as a cost reduction measure. In this type of leadframes, an Alloy 42 leadframe is first plated with a layer of nickel and gold is plated over the nickel layer. The nickel layer is used as an intermediate layer to prevent diffusion and to improve adhesion of the gold to the Alloy 42 during the plating process. In an effort to reduce plated leadframe costs further, silver was substituted for gold over a thin copper spot-plating or "strike." The copper layer is applied so that the silver plating would adhere better to the leadframe. Thus typically, the thickness of the copper layer is of the order of 5 microinches and not more than 10 microinches. The copper layer is applied only for better silver adhesion. When the copper layer is as thin as 5 microinches, particularly in

comparison with the **thick Alloy 42 leadframe,** the copper layer does not
appreciably reduce self-inductance.

US-PAT-NO: 6400569

DOCUMENT-IDENTIFIER: US 6400569 B1

TITLE: Heat dissipation in lead frames

---------- KWIC ---------

Each lead frame has a plurality of lead fingers for connection to the die
bonding pads. The lead fingers typically are **spot plated with palladium,** gold
or silver. The conductive leads are plated to provide a metallic surface to
which wires may be bonded, as a bond wire usually will not stick directly to
lead frame material, such as copper or nickel or alloys thereof.

US-PAT-NO: 6194777

DOCUMENT-IDENTIFIER: US 6194777 B1

TITLE: Leadframes with selective palladium plating

---------- KWIC ---------

Another feature of the invention provides that there is a 1 microinch layer of **palladium** over the entire surface of the lead frame, and that an additional 2 microinches is **spot plated** on the external leads from the dam bar location. In yet another aspect, **spot plating** of 2 microinches of **palladium** is applied to the external leads, and then full lead frame is flood plated with 1 microinch of **palladium**.

It is still further a feature of the present invention that **spot plated** **palladium on palladium** provides a uniform material composition and any thickness nonuniformity, such as from bleed at the spot edge interface is acceptable from adhesion or cosmetic aspects, and in turn results in relaxed specifications for spot placement.

Those devices requiring 3 microinches of **palladium** on both sides will be reversed in exposure pattern and subjected to the **spot plating** assembly a second time. The plated leadframe is cut and offset to complete the fabrication processes.

US-PAT-NO: 5459103

DOCUMENT-IDENTIFIER: US 5459103 A

TITLE: Method of forming lead frame with strengthened encapsulation adhesion

---------- KWIC ---------

This invention relates to a process for strengthening the adhesive bond between a lead frame and a plastic mold compound (350). The process involves plating the lead frame with a copper strike and selectively exposing the copper strike to an oxidizing agent to form a layer of cupric oxide (CuO) (318). Such lead frames are fitted with chips (324) and then encapsulated in the plastic mold compound (350), whereby the adhesive bond forms directly between the layer of CuO (318) and the plastic mold compound (350). A lead frame produced by this process may include a plurality of leads (310) having lead ends (312) and lead fingers (314) and a die pad (320) having a layer of CuO (318). The die pad (320) is encased by a plastic mold compound (350) which forms an adhesive bond directly with the layer of CuO (318). This layer (318) may have a thickness in a range of about 5 to 50.mu. inches (12.7 to 127 .mu.cm). Lead ends (312) and lead fingers (314) may be **spot-plated** with silver or **palladium**.

In the packaging of semiconductor IC devices, lead ends and lead fingers of the lead frame may be **spot-plated** or strike-plated with a highly conductive metal including a precious metal, such as silver, gold, or **palladium**, in order to increase the conductivity of connections between a chip and

the lead fingers or
between the lead ends of IC devices. Referring to FIG. 2, a single lead frame
200 is shown which includes leads 210, a die pad 220, and tie straps 230.
Leads 210 may be stamped or etched from a strip of lead frame material, such as
copper, and have lead ends 212 and lead fingers 214. Lead frames, such as lead
frame 200, may be manufactured in long strips in a reel-to-reel or batch
plating process.

US-PAT-NO: **6150712**

DOCUMENT-IDENTIFIER: US 6150712 A

TITLE: Lead frame for semiconductor device, and semiconductor device

---------- KWIC ---------

Disclosed are a lead frame for a semiconductor device, and a semiconductor device using the lead frame. **Inner leads** and outer leads of the lead frame are formed to have such a sectional structure that a film of **Pd or a Pd** alloy is formed on both surfaces or a rear surface of a lead frame directly or through an undercoat, and an Au-plated film is formed on a part of the film of **Pd or a Pd** alloy. Pd and Au are not applied to unnecessary areas, thus resulting in higher economical and production efficiency. The lead frame has good quality, is economical and has superior productivity. Wires connecting a semiconductor chip and the inner leads have a good connection property and joint portions of the outer leads to an external device also have a good connection property.

FIG. 2 is a fragmentary schematic sectional view showing connection between the outer lead and a base plate in the semiconductor device according to the embodiment. More specifically, in FIG. 2, an IC chip 12 disposed on the die pad 1 is connected to the inner lead 2 by a bonding wire 13, and these members are sealed off by a molding resin 14. A lower surface of a bent distal end 3a of the **outer lead** 3 extending out of the molding resin 14 is connected to the base plate 11 by soldering or a **solder** 10.

FIG. 3 shows a first embodiment of the lead frame. An essential feature of the first embodiment is illustrated in FIG. 3 which shows a sectional structure of a part of the outer lead 3 shown in FIG. 2. In the first embodiment, the die pad 1 and the guide rail 4 are each formed to have material surfaces exposed, as seen from a sectional view of FIG. 4. A film of **Pd or a Pd** alloy 7 is formed on only the **inner lead** 2 and the outer lead 3 directly or through an undercoat 6 on both sides. Then, a thin Au-plated film 8 is formed on the film 7 of Pd or a Pd alloy in a part of the outer lead 3 on both sides.

With the first embodiment, the following advantages are obtained. Since the Au-plated film 8 is not present on the die pad 1, adhesion between the die pad 1 and the molding resin 14 is improved, and wires connecting the semiconductor chip and the inner lead exhibit a better wire bonding property correspondingly. Also, since **Pd** and Au used on only the **inner lead** 2 and the outer lead 3, expensive **Pd** and Au are employed in smaller amount while ensuring a good soldering property. As a result, the lead frame according to the first embodiment can be manufactured more inexpensively than the lead frame in the related art.

US-PAT-NO: **5994212**

DOCUMENT-IDENTIFIER: US 5994212 A

TITLE: Semiconductor device and method of manufacturing the same

---------- KWIC ----------

In another aspect of the semiconductor device, the body of the **inner lead** portion is preferably made from a copper plate, the stacked plate layers of the **inner lead** portion are preferably formed by successively stacking a nickel plate layer, a **palladium** plate layer and a gold plate layer, and the metal wire is preferably made from a material including gold as a main component.

In this manner, a peeled area can be prevented from being formed in the **inner lead** portion including the **palladium** plate layer, which is poor in corrosiveness.

The third method of manufacturing a semiconductor device of this invention comprises a step of preparing a semiconductor chip having an electrode pad; a step of preparing a lead frame including an **inner lead** portion and an outer lead portion and formed by successively stacking a nickel plate layer, a **palladium** plate layer and a gold plate layer on a body of a metal; a first bonding step of bonding the electrode pad with a metal wire made from a material including gold as a main component, with a tip of the metal wire placed on the electrode pad of the semiconductor chip, with applying a load and ultrasonic waves; and a second bonding step of bonding the

metal wire onto the
inner lead portion with another part of the metal wire
placed on the **inner lead**
portion, with applying a load of 150 through 250 g and
ultrasonic waves with a
power of 0 through 20 mW.

said stacked plate layers of said **inner lead** portion are
formed by successively
stacking a nickel plate layer, a **palladium** plate layer and
a gold plate layer,
and

a step of preparing a lead frame including an **inner lead**
portion and an outer
lead portion and formed by successively stacking a nickel
plate layer, a
palladium plate layer and a gold plate layer on a body of a
metal;

US-PAT-NO: **5804468**

DOCUMENT-IDENTIFIER: US 5804468 A

TITLE: Process for manufacturing a packaged semiconductor having a divided leadframe stage

---------- KWIC ---------

In step ST2, a plating process is performed in which the aforementioned SnNi protection film is coated on the outer leads 257b. Further, at least the end portions of the **inner leads** 253a and the chip-mounting-side surfaces of the second and third areas 253b and 253c are plated with a metallic film suitable for wire bonding, such as silver (Ag), gold (Au) or **palladium (Pd)**.

In step ST15, the back surface of the stage 253 exposed from the package 259 is removed by a chemical etching process until the half-etched grooves 253 appear. Thereby, as shown in FIG. 17C, the first, second and third areas 253a, 253b and 253c are completely separated from each other by the resin. In the above chemical etching process, the assembly is placed in an etchant. It will be noted that the outer leads 257b are plated with SnNi and the outer leads 257b are not etched. In step ST16, the **outer leads** 257b are plated with **solder**. In step ST17, the outer leads 257b are bent in the gull-wing shape.

FIG. 20 is a diagram of a method of producing the semiconductor device 251B shown in FIG. 19. In FIG. 20, steps which are the same as those shown in FIGS. 18A and 18B are given the same reference numbers as

previously, and a description thereof will be omitted. In step S13 shown in FIG. 20, only wires connecting the semiconductor chip 254 to the second and third stage areas 253b and 253c are provided because the semiconductor device 251B employs the bump electrodes 260. The bump electrodes 260 are provided in step ST16.sub.A subsequent to step ST16 in which the **outer leads** 257b are plated with **solder**. After step ST16.sub.A, step S17 is performed.

In step ST25, the end portions of the **inner leads** 257a1-257a8 are plated with Ag, Au or **Pd**. The portions corresponding to the outer leads 257b are plated with SnNi in order to improve the anti-etching performance. In step ST26, the stage-part frame 252A and the lead-part frame 252B are stacked so that the end portions of the signal-system inner leads 257a3 adhere to the top of the insulating adhesive tape 263. In step ST27, the insulating adhesive tape 265 is cured whereby the inner leads 257a3 are fixed to the insulating adhesive tape 265. Then, by using the lead frame 252 thus formed, the semiconductor device 251E is produced in the same manner as shown in FIG. 18B.

US-PAT-NO: 6265761

DOCUMENT-IDENTIFIER: US 6265761 B1

TITLE: Semiconductor devices with improved lead frame structures

---------- KWIC ---------

The width of the outer lead portion 10 in one embodiment is between approximately 0.25 and 0.36 mm, with an approximate center-to-center spacing of 0.65 mm. The inner lead portion 12, 14 has a width between approximately 0.41 and 0.45 mm. In another embodiment, the outer lead 10 width is between approximately 0.18 and 0.27 mm, the center to center spacing is 0.50 mm, and the inner lead 12, 14 width is between approximately 0.26 and 0.30 mm. The widths of the inner lead portions are preferably controlled by making the gaps between them as small as the manufacturing process will allow, while maintaining electrical isolation. If the lead frame is manufactured with standard chemical etching techniques, the gap can be generally as small as the **lead frame is thick,** typically between 0.13 and 0.18 mm.